REMARKS

Applicants appreciate the detailed examination evidenced by the Official Action mailed September 8, 2004 (hereinafter the Official Action). In response, Applicants have amended independent Claims 1, 13, 17, and 36 to include the recitation of, for example,

> comparing a first error rate associated with the first data stream to a second error rate associated with the second data stream if the first and second error levels are acceptable,

to further clarify the claimed subject matter. As discussed herein below in greater detail, Serizawa does not disclose or suggest, among other things, determining different error levels and error rates as recited in the claims (*i.e.,* the amended as well as the unamended claims). Accordingly, Applicants respectfully request withdrawal of all rejections and the allowance of all claims for at least the reasons discussed herein.

Independent Claims 1, 13, 17, 29, and 36 are patentable over Serizawa.

Claims 1 – 23 and 25 – 41 stand rejected under 35 USC § 102 over U.S. Patent No. 5,283,531 to Serizawa et al. ("Serizawa"). *Official Action, page 2.* As discussed above, Applicants have amended some of the independent Claims to recite "comparing a first **error rate** associated with the first data stream to a second **error rate** associated with the second data stream if the first and second **error levels** are acceptable." For example, independent Claim 1 has been amended to insert in-part:

> demodulating radio signals to provide a first data stream;
> demodulating the radio signals concurrently to provide a second data stream;
> **determining a first error level** associated with the first data stream that indicates the acceptability of the first data stream for further processing;
> **determining a second error level** associated with the second data stream that indicates the acceptability of the second data stream for further processing; and
> **comparing a first error rate associated with the first data stream to a second error rate associated with the second data stream if the first and second error levels are acceptable**,

Applicants further note that unamended Claims 13 and 29 include similar recitations.

Applicants respectfully submit that Serizawa does not disclose or suggest determining separate **error levels** for the first and second data streams, and further,

comparing a first **error rate** associated with the first data stream to a second **error rate** associated with the second data stream if the first and second error levels are acceptable. In other words, Serizawa does not disclose or suggest **determining error rates in addition to error levels**.

As understood by Applicants, Serizawa discusses, for example, comparing the bit codes of the output digital signals from the first and second demodulators 102 and 104, in order to measure a rate of non-coincidence D of the bit codes. *See for example, column 8, lines 10 – 15 of Serizawa.* Accordingly, Serizawa does not appear to make a direct measurement of first and second error levels (such as the CRC error levels discussed in Applicants disclosure). To the contrary, Serizawa appears to compare the respective data streams produced by the first and second demodulators to determine the rate of noncoincidence D. The rate of noncoincidence appears to be used to draw an inference as to which demodulator may be better suited for current condition. For example, Figure 4 of Serizawa illustrates the tradeoffs between an adaptive and nonadaptive demodulator used to demodulate a signal with vary amounts of multipath delay. Point C in Figure 4 of Serizawa illustrates the point beyond which, if more multipath delay is introduced, a demodulator incorporating an adaptive equalizer may produce lower error rates compared to a demodulator that does not include adaptive equalizer.

However, as stated above, it appears to Applicants that Serizawa does not disclose direct determinations of first and second error levels associated with the outputs produced by the first and second demodulators as Serizawa. For example, Figure 3 of Serizawa appears to show a direct comparison of the outputs produced by the first and second demodulators by bit code comparison device 106. Figure 3, however, does not include any reference to direct determination of first and second error levels associated with the different demodulators. Accordingly, Applicants respectfully submit that Serizawa does not disclose or suggest first and second error levels associated with the first and second data streams respectively.

Furthermore, Serizawa also does not disclose or suggest comparing a first error rate associated with the first data stream to a second error rate associated with the second data stream if the first and second error levels are acceptable. In particular, the embodiments discussed in Serizawa do not appear to disclose or suggest this type of

multilevel error checking for determination as to which demodulator is to be used in a particular situation. To the contrary, Serizawa discusses selecting one of the modulators based on the presence or absence of a multipath delay which is determined based, for example, on the noncoincidence of bit codes, whereupon the operation of the other demodulator is stopped. *See Abstract of Serizawa.*

In contrast to Serizawa, as discussed in Applicants disclosure with reference to, for example, Figure 4:

> First and second error circuits **315, 320** are electrically coupled to the first and second deinterleavers/channel decoders **350, 355**. Class 1A bits included in the first and second data streams are provided to first and second CRC error check circuits **370, 375** included in the first and second error circuits **315, 320**. The first and second CRC error circuits **370, 375** can provide an indication of whether an acceptable/unacceptable number of errors was detected in the respective data stream. The indications of an acceptable/unacceptable number of errors in the first and second data streams are provided to the selection circuit **325**.
>
> The first and second data streams are also provided to first and second reencoder/reinterleaver circuits **360, 365** to provide first and second reconstructed data streams. The first and second reencoder/reinterleaver circuits **360, 365** nearly reverse the processing provided by the first and second deinterleavers/channel decoders **350, 355**. It will be understood that some of the error correction provided by the channel decoders discussed above may not be reversed exactly so that the reconstructed data may not match the raw data.
>
> The first and second reconstructed data streams can be provided to first and second comparison circuits **380, 385** included in the first and second errors circuits **315, 320**. The first and second comparison circuits **380, 385** can compare the raw data streams to the reconstructed data streams to provide an indication of how many of the bits in the first and second raw data streams were in error. In some embodiments, the first and second comparison circuits **380, 385** can be used to determine which of the data bits in a frame were in error. The number of bits in error and which bits were in error in each of the data streams can be provided to the selection circuit **325**.
>
> The first and second comparison circuits **380, 385** can be first and second bit error rate circuits **315, 320**. The bit error rate circuits can determine the rate at which errors occurred as a fraction of some unit of data or time. For example, the bit error rate can be expressed as N errors/second or N errors/MB. Bit error rate calculations are well known

> in the art and need not be discussed further herein. *Application, page 9, lines 26 – 33, page 10, lines 1 – 21.*

As demonstrated by the above cited passages of Applicants disclosure, the embodiments disclosed therein can include the **determination of both error levels and error rates** (such as CRC determinations and bit error rates determination respectively), which is not disclosed or suggested by Serizawa.

Accordingly, independent Claims 1, 13, 17, 29, and 36 are patentable over Serizawa for at least the reasons discussed above. Furthermore dependent Claims – 2-12, 14-16, 18-28, and 30-35 are patentable at least per the patentability of the independent claims from which they depend.

Many of the dependent claims are separately patentable over Serizawa.

In addition to the reasons discussed above with reference to the independent claims, many of the dependent claims provide separate bases for patentability over Serizawa. For example, Serizawa does not disclose or suggest the recitations of Claim 5:

> wherein one of the first and second data streams comprises a previously selected data stream, wherein the method further comprises selecting the previously selected data stream if the first and second error rates are about equal.

As understood by Applicants, no part of Serizawa discusses selecting a previously selected data stream if the first and second error rates are about equal. As discussed above in reference to the independent claims, Serizawa does not determine separate error levels and error rates. Moreover, Serizawa does not disclose or suggest selecting a previously selected data stream (*i.e.* the use of one modulator or the other) if the error rates are about equal to one another. For example, as discussed in Applicants disclosure:

> If the CRC check on the first data stream indicates an acceptable error level (block **405**) and the CRC check on the second data stream also indicates an acceptable error level (block **410**), or if neither CRC check indicates an acceptable error level (blocks **405,420**), the raw bit error rates for the re-encoded first and second data streams (block **430**) can be used to select the data stream. If the bit error rates for the first and second data streams are about equal (block **435**), the previously selected data stream can be selected for further processing and the selected data stream is designated as the previously selected data stream (block **440**).

> If the bit error rate associated with the first data stream is greater than the bit error rate associated with the second data stream (block **445**), the second data stream can be selected for further processing and the second data stream can be designated as the previously selected data stream (block **425**). On the other hand, if the bit error rate associated with the first data stream is less than the bit error rate associated with the second data stream (block **445**), the first data stream can be selected for further processing and the first data stream can be designated as the previously selected data stream (block **415**). *Application, page 12, lines 1 – 16.*

As demonstrated by the above-cited passage of Applicants disclosure, embodiments therein can select a previously selected demodulator for use if the error rates for the first and second data streams are about equal. Accordingly, dependent Claims 31 and 40 are patentable for at least these additional reasons.

CONCLUSION

Applicants have amended selected independent claims and have shown that these recitations are not disclosed or suggested by Serizawa. Accordingly, Applicants respectfully request the withdrawal of all rejections and the allowance of all claims in due course. If any informal matters arise, the Examiner is encouraged to contact the undersigned by telephone.

Respectfully submitted,

Robert N. Crouse
Registration No. 44,635

USPTO Customer No. 20792
Myers Bigel Sibley & Sajovec
Post Office Box 37428
Raleigh, North Carolina 27627
Telephone: 919/854-1400
Facsimile: 919/854-1401

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Audra Wooten